DATA INPUT AND OUTPUT CIRCUITS FOR
MULTI-DATA RATE OPERATION

ABSTRACT OF THE DISCLOSURE

5   Data input and output circuits that support multi data rate and a number of

timing schemes. In one design, a data output circuit includes an input multiplexer, data

latches, an output multiplexer, and at least one output driver. The input multiplexer receives

a set of data bits in a first order (e.g., odd and even) and provides the data bits in a second

order (e.g., first and second). The data latches can latch the data bits with (1) a latch signal to

10   satisfy memory access timing requirements and (2) a data write clock signal to satisfy output

timing requirements. The output multiplexer multiplexes the latched data bits to provide time

multiplexed data bits. The output driver(s) provide signal drive for the time multiplexed data

bits. Clock signals with various timing characteristics can be used to allow the data output

circuit to satisfy various timing requirements.